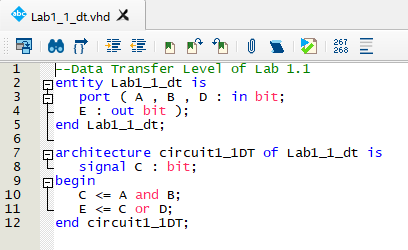
**Name: Date:** Jan 27th 2023

Umama Rahman (ID: 202000915)

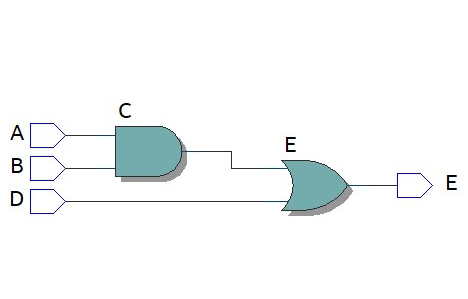
Shair Yousuf Jahin (ID: 202018305)

**1.1 Task 1: Intro to VHDL code**

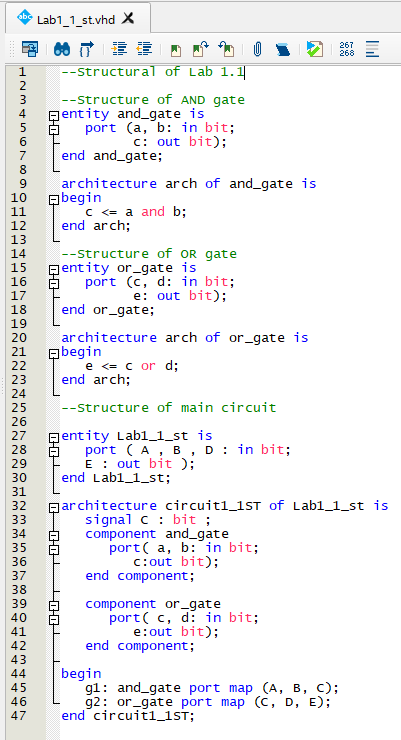
* Dataflow (RTL level) Code:



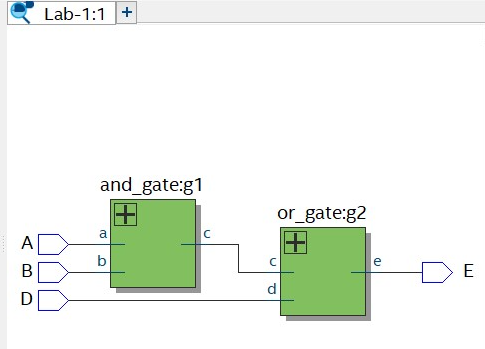
Dataflow - RTL Simulation view:



* Structural (Gate level) Code:

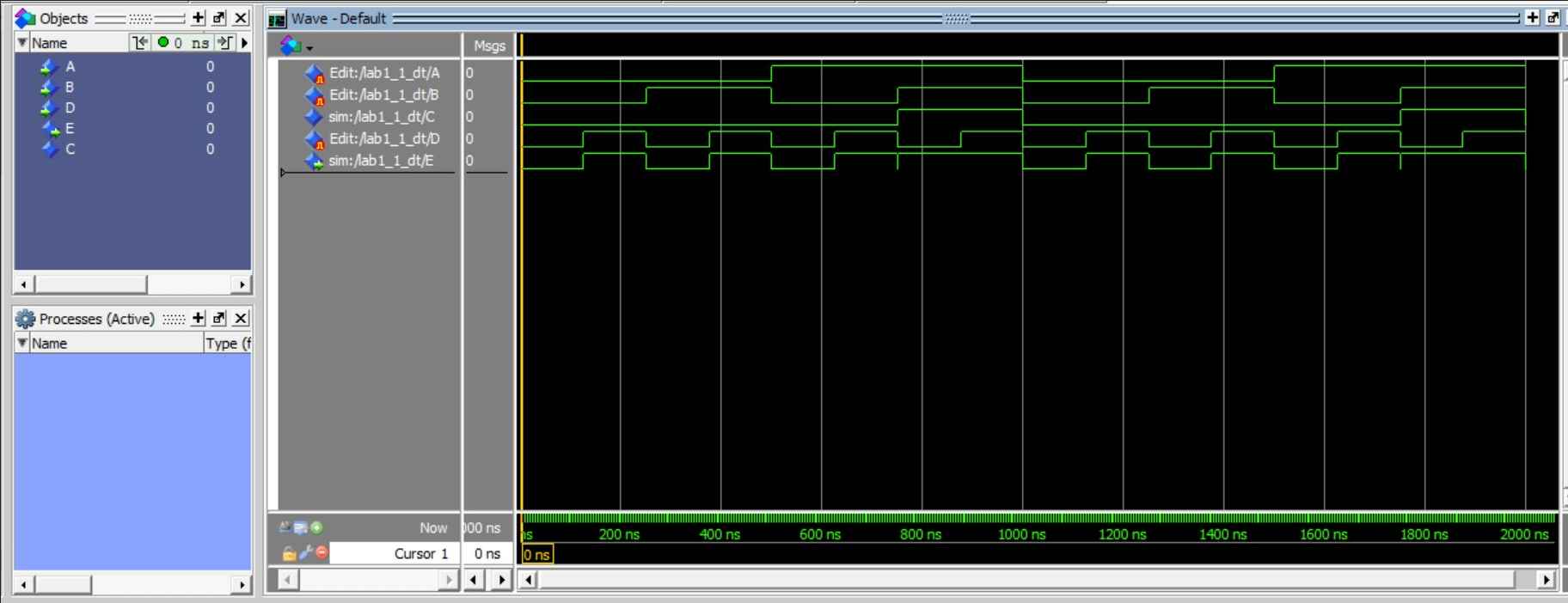


Structural RTL simulation view:



**1.2 Simulation Labratory**

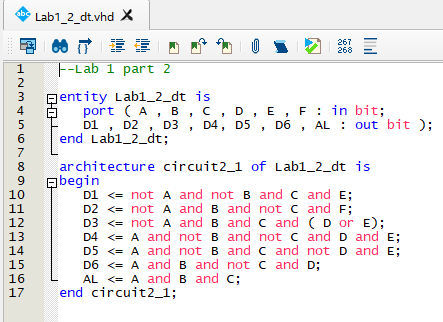
Used QuestaSim to simulate the waveforms to test the inputs and outputs of the circuit

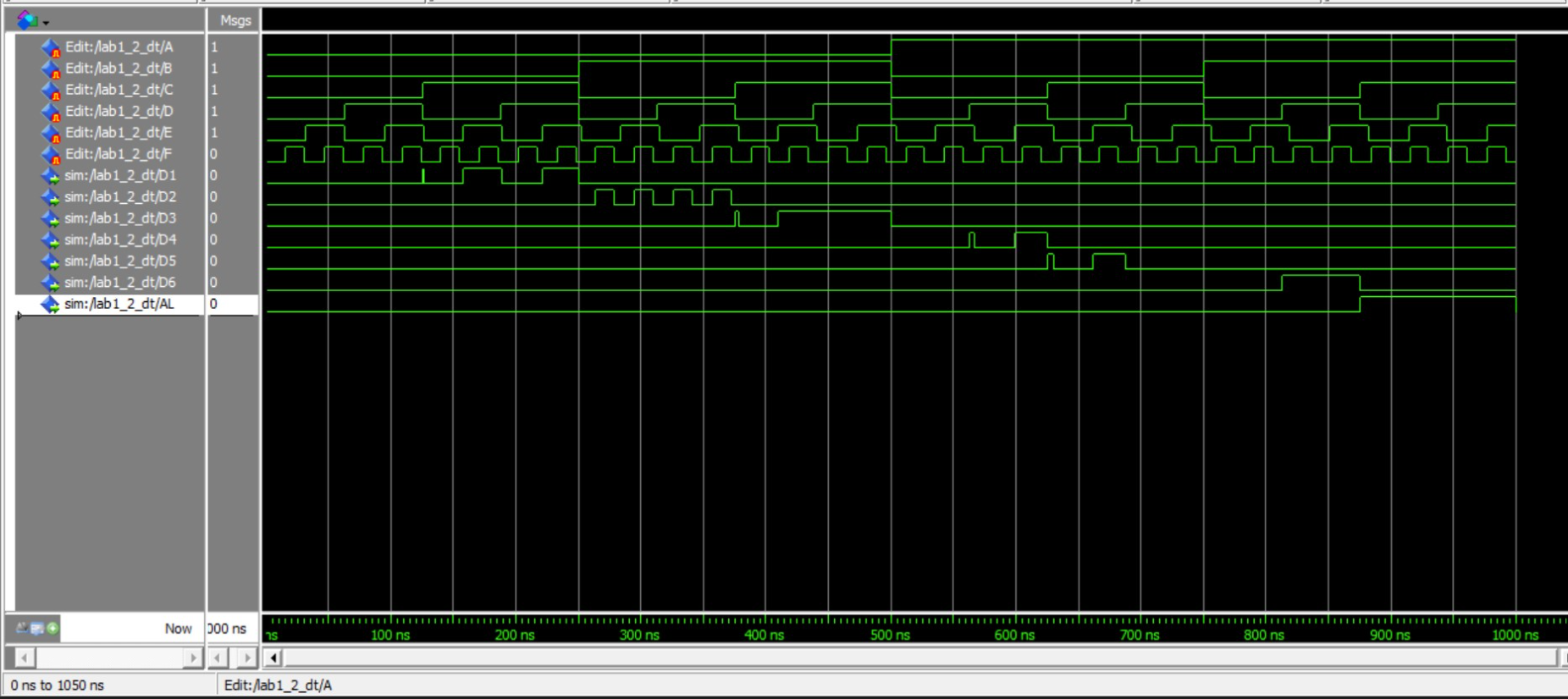


**Task 2. Combinational Logic Design Using VHDL**

**2.2 Simulation Laboratory**

VHDL code for combinational logic for system using prelab:



Waveforms generated with multiple combinations of A, B, C, D, E and F to simulate the system and test code with six inputs and seven outputs:

**1. Comment on the success of the lab. Were the results as expected? What problems were encountered and how were they overcome?**

The lab was successfully completed in the allotted time. We could compare our results with our prelab and get the expected results. The circuit diagrams also matched the RTL simulations made from our VHDL code. We tested the Task 2 combinational logic circuit design using all the possible combinations for A, B, C, D, E and F inputs to get the different outputs.

We were unable to use the University program VWF on the laptop we were doing the lab on, so we used QuestaSim to generate waveforms to do the testing of our circuit designs.

**2. State and comment on the major learning outcomes of the experiment**

The major learning outcomes of the experiment were good comprehension of VHDL code implementation in Quartus and developing the testing of the VHDL code using a waveform generator to test various inputs and observe the output waveform.

We also were able to implement our Digital logic knowledge to work on the pre-lab and then were able to develop familiarity with using the Quartus application.